IMPROVING ELECTROSTATIC DISCHARGE PERFORMANCE OF A SILICON STRUCTURE AND EFFICIENT USE OF AREA WITH ELECTROSTATIC DISCHARGE PROTECTIVE DEVICE UNDER THE PAD APPROACH AND ADJUSTMENT OF VIA CONFIGURATION THERETO TO CONTROL DRAIN JUNCTION RESISTANCE

ABSTRACT

More efficient use of silicon area is achieved by incorporating an electrostatic discharge protective (ESDP) device beneath a pad area of a semiconductor structure. The pad area includes a substrate having a first metal layer above it. A second metal layer is above the first metal layer. The ESDP device resides in the substrate below the first metal layer. A layer of dielectric separates the first and second metal layers. A via within the dielectric layer electrically couples the first and second metal layers. A via connects to the ESDP component. Subsequent metal layers can be arranged between the first and second metal layers. The Ohmic value of the resistance component of the ESDP device can be set during fabrication by fixing a number of individual via components, arranged electrically in parallel, by fixing the cross sectional area of the via components, and/or by fixing the length of the via components.